1.1W Mono Low-Voltage Audio Power Amplifier

Features

- Operating Voltage : 2.6V-5.5V
- APA0710 Compatible with TPA711
  APA0711 Compatible with TPA751
- Bridge-Tied Load (BTL) or Single-Ended (SE) Modes Operation (for APA0710 only)
- Supply Current
  – I_{DD}=1.3mA at V_{DD}=5V ,BTL mode
  – I_{DD}=0.9mA at V_{DD}=3.3V ,BTL mode
- Low Shutdown Current
  – I_{DD}=0.1μA
- Low Distortion
  – 630mW, at V_{DD}=5V, BTL, R_L=8Ω THD+N=0.15%
  – 280mW, at V_{DD}=3.3V, BTL, R_L=8Ω THD+N=0.15%
- Output Power
  at 1% THD+N
  – 900mW, at V_{DD}=5V, BTL, R_L=8Ω
  – 400mW, at V_{DD}=3.3V, BTL, R_L=8Ω
  at 10% THD+N
  –1.1W at V_{DD}=5V, BTL, R_L=8Ω
  –480mW at V_{DD}=3.3V, BTL, R_L=8Ω
- Depop Circuitry Integrated
- Thermal Shutdown Protection and Over Current Protection Circuitry
- High supply voltage ripple rejection
- Surface-Mount Packaging
  – 8 pin MSOP-P (with enhanced thermal pad) power package available
  – SOP-8 package
- Lead Free Available (RoHS Compliant)

General Description

The APA0710 is a bridged-tied load (BTL) or singled-ended (SE) audio power amplifier developed especially for low-voltage applications where internal speakers and external earphone operation are required. The APA0711 is a only BTL audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 5V supply, the APA0710/1 can deliver 1.1W of continuous power into a BTL 8Ω load at 10% THD+N throughout voice band frequencies. Although this device is characterized out to 20kHz,its operation is optimized for narrow band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. A unique feature of the APA0710 is that it allows the amplifier to switch from BTL to SE on the fly when an earphone drive is required. This eliminates complicated mechanical switching or auxiliary devices just to drive the external load. This device features a shutdown mode for power-sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The APA0710/1 are available in an 8-pin SOP and 8-pin MSOP-P with enhanced thermal pad.

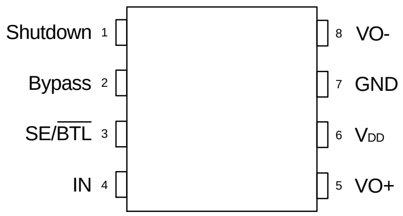
Applications

- Mobil Phones
- PDAs
- Digital Camera
- Portable Electronic Devices

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

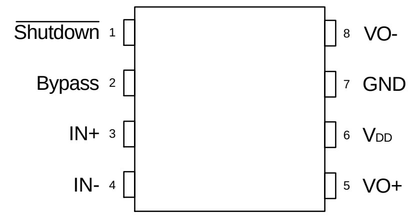
Pin Description

APA0710



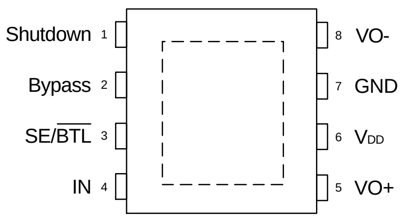
SOP-8

APA0711



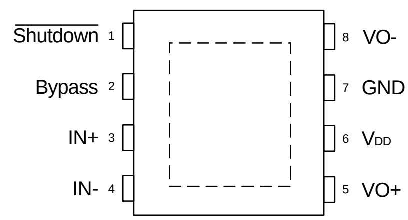
SOP-8

APA0710



MSOP-8-P

APA0711



MSOP-8-P

NC = No internal connection

= Thermal Pad

(connected to GND plane for better heat dissipation)

Ordering and Marking Information

APA0710/1 □□-□□ □ Lead Free Code Handling Code Temp. Range Package Code	Package Code K : SOP-8 XA : MSOP-8-P Temp. Range I : -40 to 85 °C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APA0710/1 K : APA0710/1 XXXXX	XXXXX - Date Code
APA0710/1 XA : A0710/1 XXX XX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

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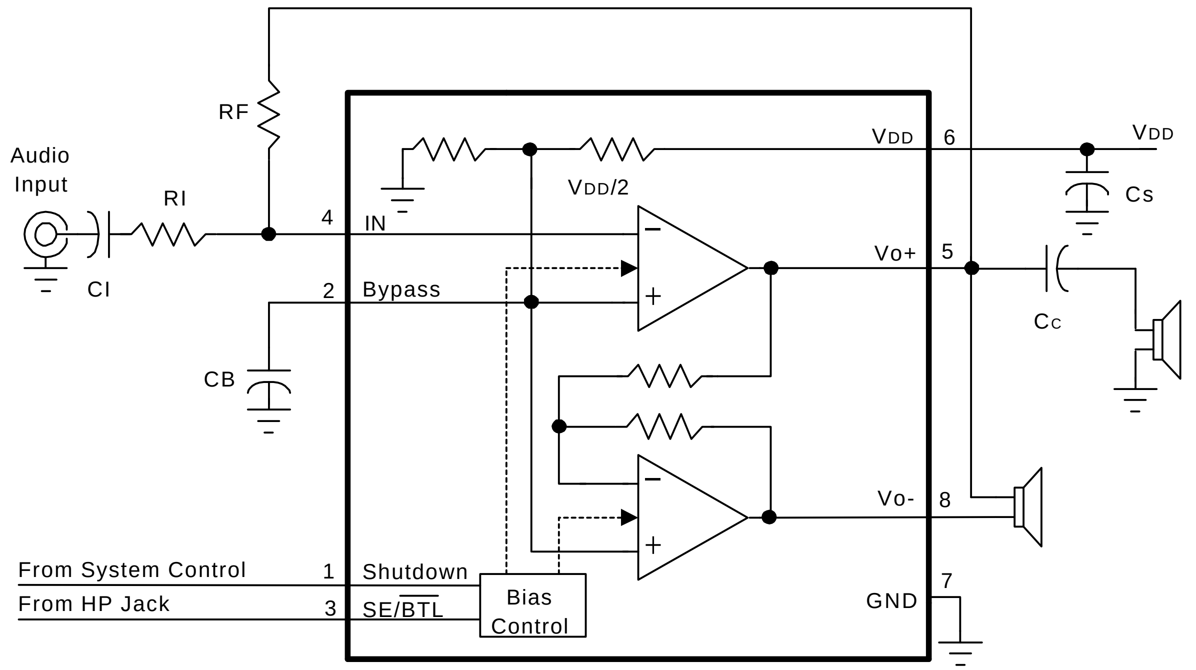
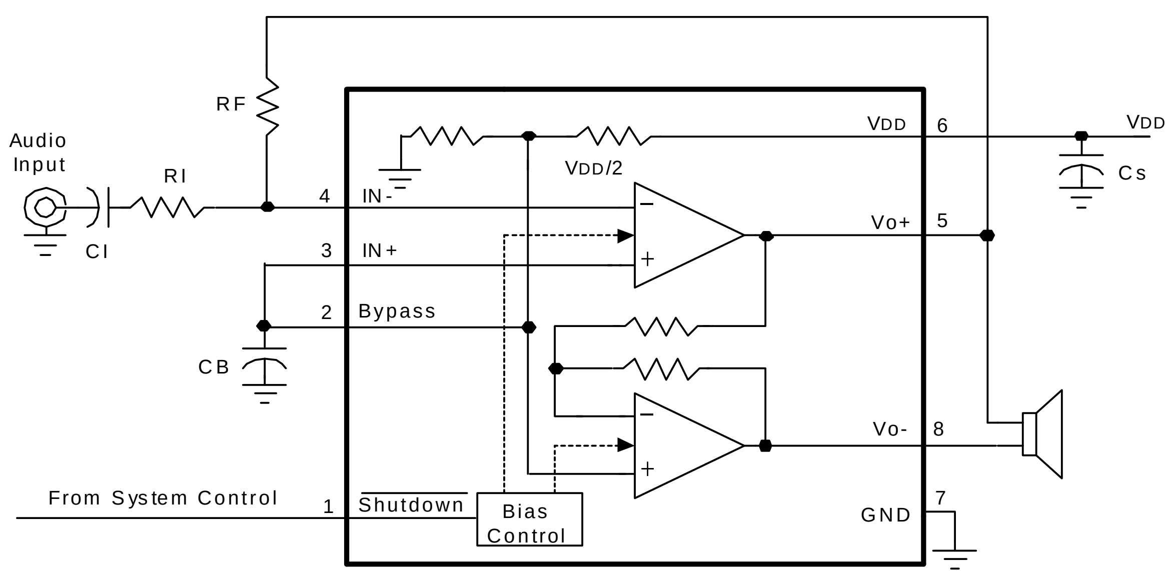
Block Diagram



APA0710



APA0711

Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}	Input Voltage Range, Shutdown, SE/$\overline{\text{BTL}}$	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Internally Limited*[1]	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature, 10 seconds	260	°C
V_{ESD}	Electrostatic Discharge	-2000 to 2000*[2]	V
P_D	Power Dissipation	Internally Limited	W

Note:
1.APA0710/1 integrated internal thermal shutdown protection when junction temperature ramp up to 170°C
2.Human body model: C=100pF, R=1500Ω, 3 positives pulses plus 3 negative pulses
3.Machine model: C=200pF, L=0.5µF, 3 positive pulses plus 3 negative pulses

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		2.6	5.5	V
V_{IH}	High-Level Voltage	Shutdown, $\overline{\text{Shutdown}}$	2.2		V
		SE/$\overline{\text{BTL}}$	0.9V_{DD}		
V_{IL}	Low-Level Voltage	Shutdown, $\overline{\text{Shutdown}}$		0.4	V
		SE/$\overline{\text{BTL}}$		0.9V_{DD}-1	

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air		°C/W
	MSOP-8-P*	50	
	SOP-8	160	

* 3.42in^2 printed circuit board with 20z trace and copper through 6 vias of 12mil diameter vias.
The thermal pad on the MSOP-8-P package with solder on the printed circuit board.

Electrical Characteristics

Electrical Characteristics at Specified Free - Air Temperature

V_{DD} = 3.3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA0710/1			Unit
			Min.	Typ.	Max.	
V_{OO}	Output Offset Voltage	R_L = 8Ω, R_F = 10kΩ			20	mV
I_{DD}	Supply Current	BTL mode, R_F = 10kΩ		0.9	1.8	mA
		SE mode, R_F = 10kΩ		0.55	1.1	
$I_{DD(SD)}$	Supply Current, Shutdown Mode	R_F = 10kΩ		0.1	2	μA
|IH|		Shutdown, $V_I = V_{DD}$			1	μA
		$\overline{\text{Shutdown}}$, $V_I = V_{DD}$			1	
		SE/$\overline{\text{BTL}}$, $V_I = V_{DD}$			1	
|IL|		Shutdown, V_I = 0V			1	μA
		$\overline{\text{Shutdown}}$, V_I = 0V			1	
		SE/$\overline{\text{BTL}}$, V_I = 0V			1	
Operating characteristic, V_{DD} = 3.3V, T_A = 25°C, RL = 8W						
P_O	Output Power (Note 1)	THD = 1%, BTL mode, R_L = 8Ω		400		mW
		THD = 1%, SE mode, R_L = 32Ω		40		
THD+N	Total Harmonic Distortion Plus Noise (Note 1)	P_O = 280mW, BTL mode, R_L = 8Ω		0.15		**%**
Bom	Maximum Output Power Bandwidth	Gain = 2, THD+N = 2%		20		kHz
B1	Unity-Gain Bandwidth	Open Loop		2		MHz
PSRR	Power Supply Rejection Ratio (Note1)	C_B = 1μF, BTL mode, R_L = 8Ω		74		dB
		C_B = 1μF, SE mode, R_L = 8Ω		61		
Vn	Noise Output Voltage	Gain = 1, C_B = 0.1μF		28		μV(rms)
T_{WU}	Wake-up time	C_B = 1μF		380		ms

V_{DD}= 5V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA0710/1			Unit
			Min.	Typ.	Max.	
V_{OO}	Output Offset Voltage	R_L = 8Ω, R_F = 10kΩ			20	mV
I_{DD}	Supply Current	BTL mode, R_F = 10kΩ		1.3	2.6	mA
		SE mode, R_F = 10kΩ		0.75	1.5	
$I_{DD(SD)}$	Supply Current , Shutdown Mode	R_F = 10kΩ		0.1	2	μA

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Electrical Characteristics(Cont.)

Electrical Characteristics at Specified Free - Air Temperature (Cont.)

V_{DD}= 5V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA0710/1			Unit
			Min.	Typ.	Max.	
|IH|		Shutdown, $V_I = V_{DD}$			1	µA
		$\overline{\text{Shutdown}}$, $V_I = V_{DD}$			1	
		SE/$\overline{\text{BTL}}$, $V_I = V_{DD}$			1	
|IL|		Shutdown, V_I = 0V			1	µA
		$\overline{\text{Shutdown}}$, V_I = 0V			1	
		SE/$\overline{\text{BTL}}$, V_I = 0V			1	
Operating characteristic, V_{DD} = 5V, T_A = 25°C, R_L = 8W						
P_O	Output Power (Note 1)	THD = 1%, BTL mode, R_L = 8Ω		900		mW
		THD = 1%, SE mode, R_L = 32Ω		94		
THD+N	Total Harmonic Distortion Plus Noise (Note 1)	P_O = 630mW, BTL mode, R_L = 8Ω		0.15		%
Bom	Maximum Output Power Bandwidth	Gain = 2, THD+N = 2%		20		kHz
B1	Unity-Gain Bandwidth	Open Loop		2		MHz
PSRR	Power Supply Rejection Ratio (Note1)	C_B = 1µF, BTL mode, R_L = 8Ω		74		dB
		C_B = 1µF, SE mode, R_L = 8Ω		61		
Vn	Noise Output Voltage	Gain = 1, C_B = 0.1µF		28		µV(rms)
Twu	Wake-up time	C_B = 1µF		400		ms

Note1 : Output power is measured at the output terminals of device at f=1KHz.

Pin Description

APA0710

Pin		I/O	Description
Name	No		
Shutdown	1	I	Shutdown mode control signal input, place entire IC in shutdown mode when held high.
Bypass	2	I	Bypass pin
SE/$\overline{\text{BTL}}$	3	I	When SE/$\overline{\text{BTL}}$ is held low, the APA0710 is in BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the APA0710 is in SE mode
IN	4	I	In is the audio input terminal
VO+	5	O	VO+ is the positive output for BTL and SE modes
V_{DD}	6		Supply voltage input pin
GND	7		Ground connection for circuitry
VO-	8	O	VO- is the negative output in BTL mode and a high-impedance output in SE mode

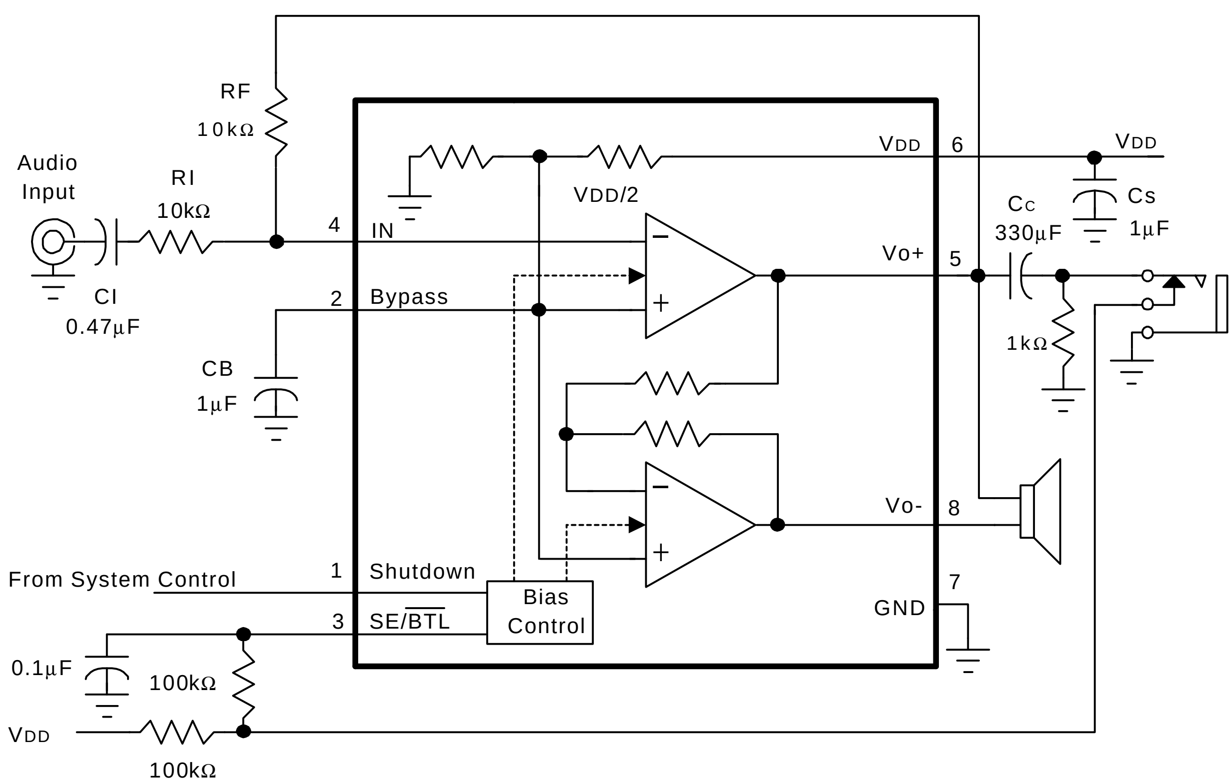
Pin Description

APA0711

Pin		I/O	Description
Name	No		
$\overline{\text{Shutdown}}$	1	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.
Bypass	2	I	Bypass pin
IN+	3	I	IN+ is the non-inverting input. IN+ is typically tied to the Bypass terminal.
IN-	4	I	IN- is the inverting input. IN- is typically used as the audio input terminal.
VO+	5	O	VO+ is the positive BTL output.
V_{DD}	6		Supply voltage input pin.
GND	7		Ground connection for circuitry.
VO-	8	O	VO- is the negative BTL output.

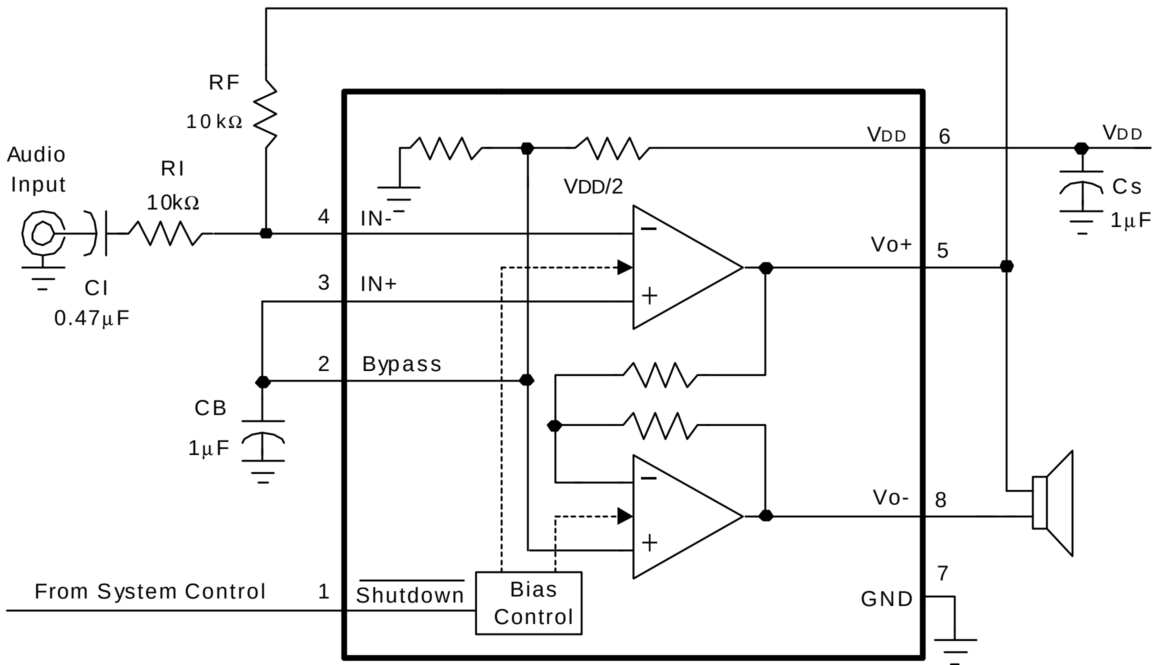
Typical Application Circuit

for APA0710 Application

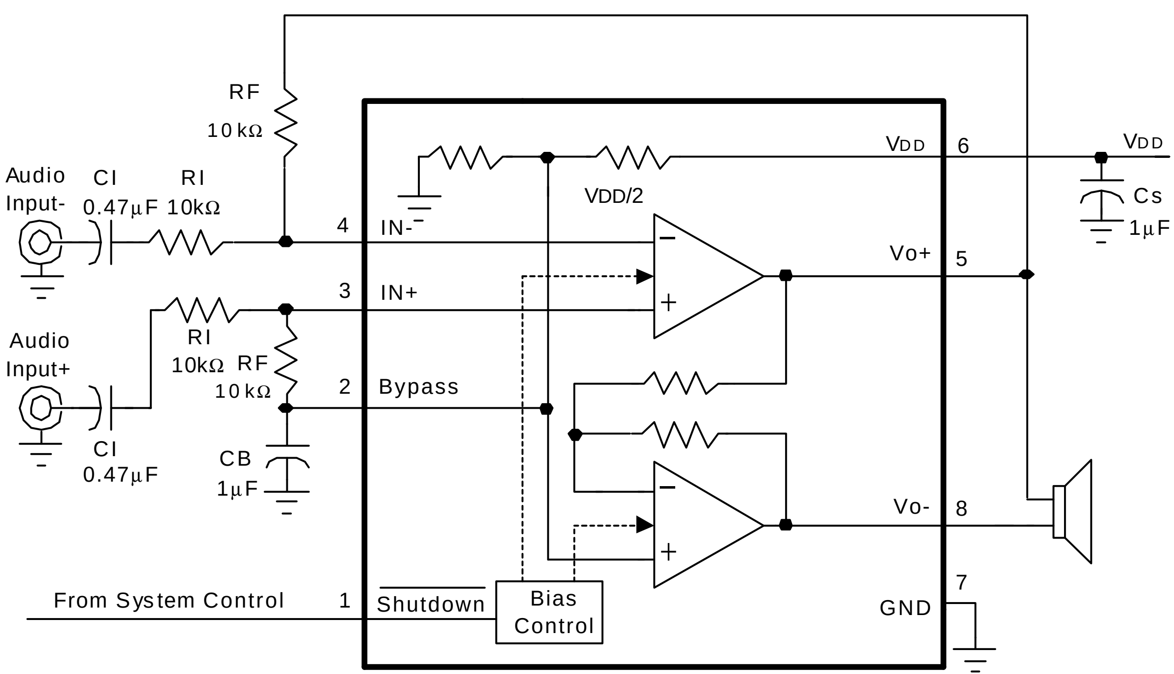


Typical Application Circuit (Cont.)

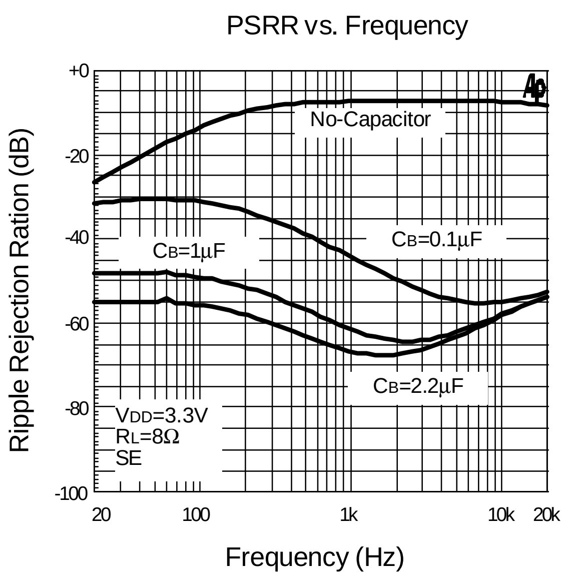
for APA0711 Application

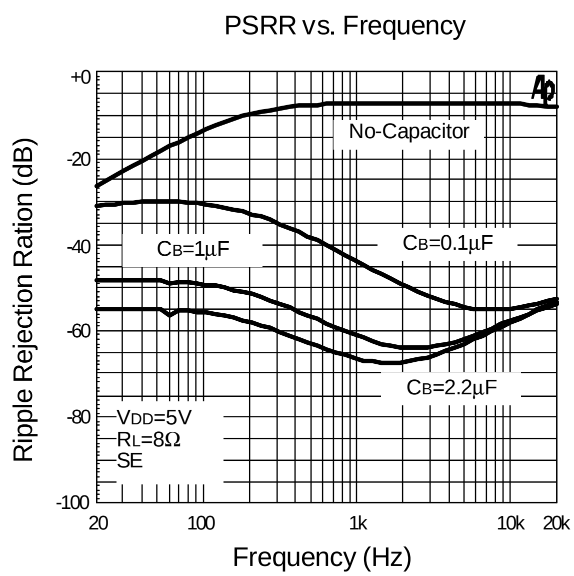


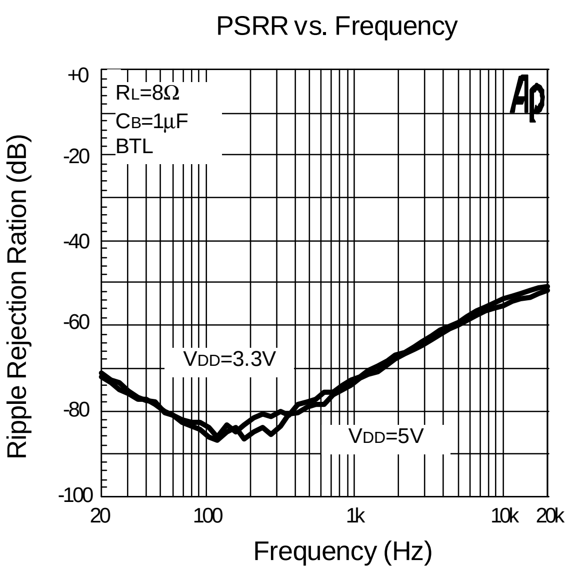
for APA0711 Differential Input Application

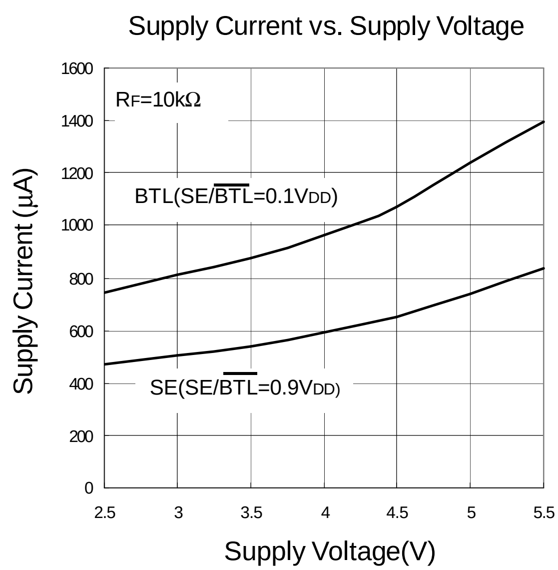


Typical Characteristics



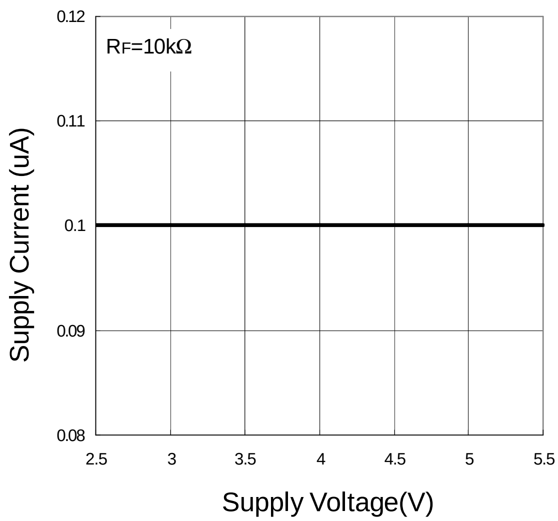




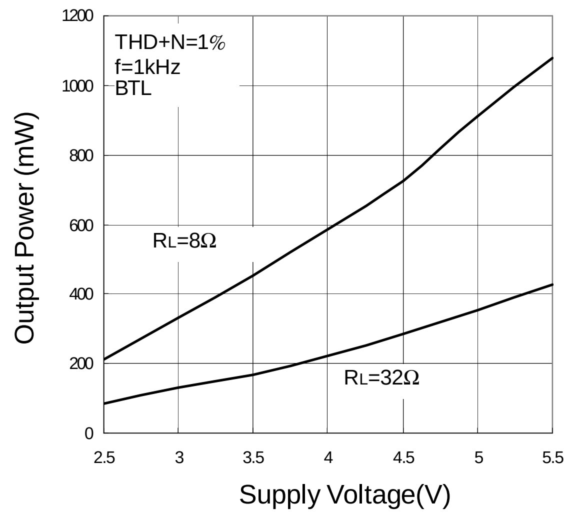


Typical Characteristics (Cont.)

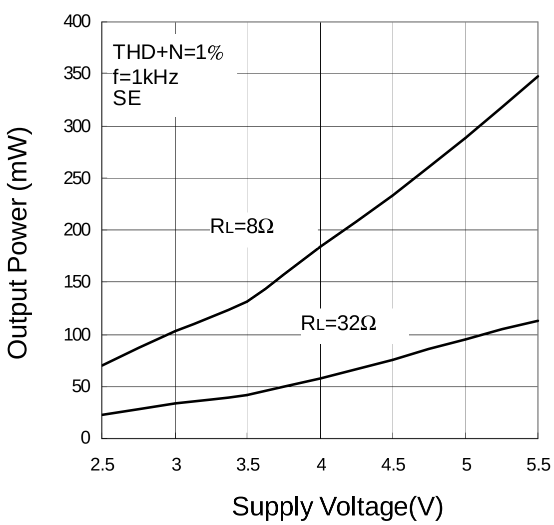
Supply Current vs. Supply Voltage



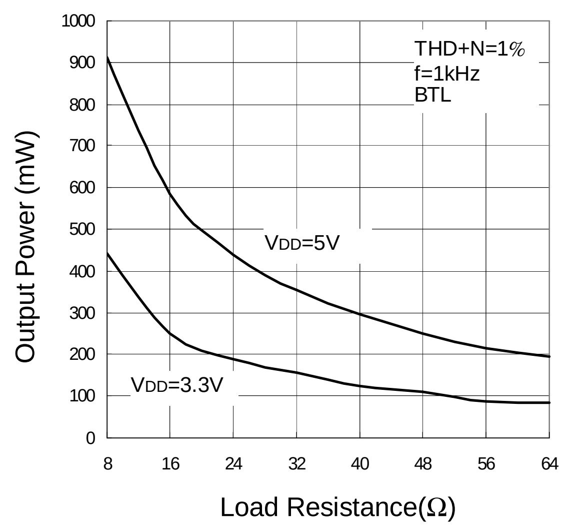
Output Power vs. Supply Voltage



Output Power vs. Supply Voltage



Output Power vs. Load Resistance



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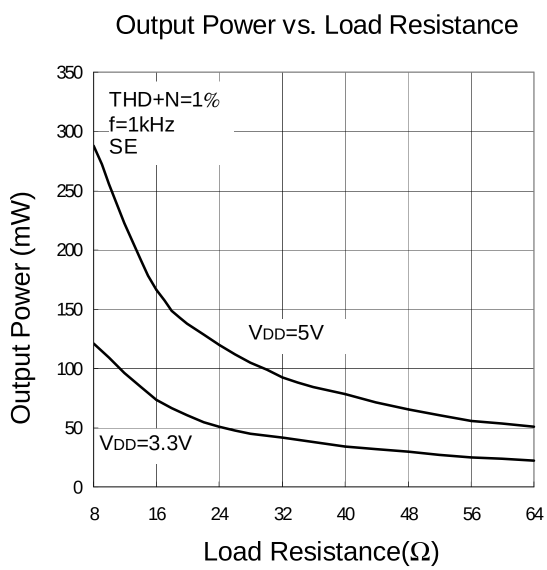
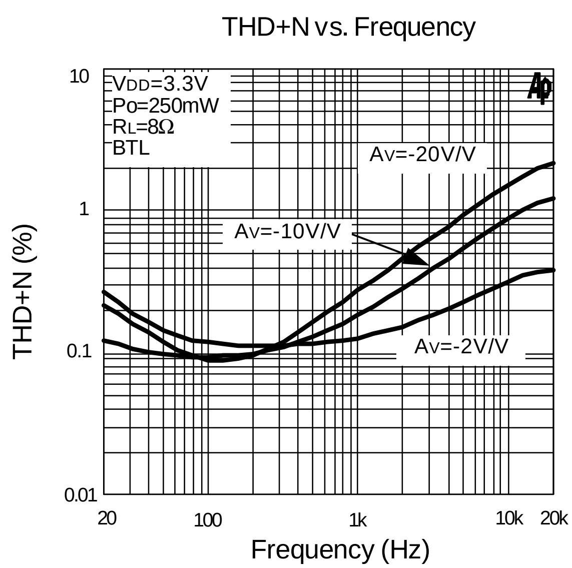
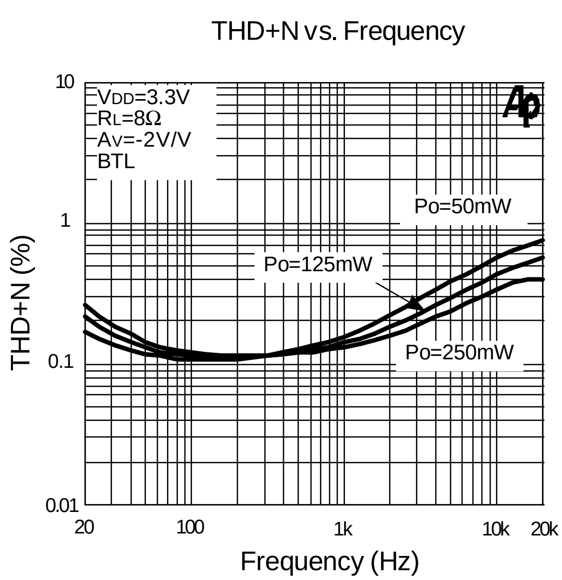
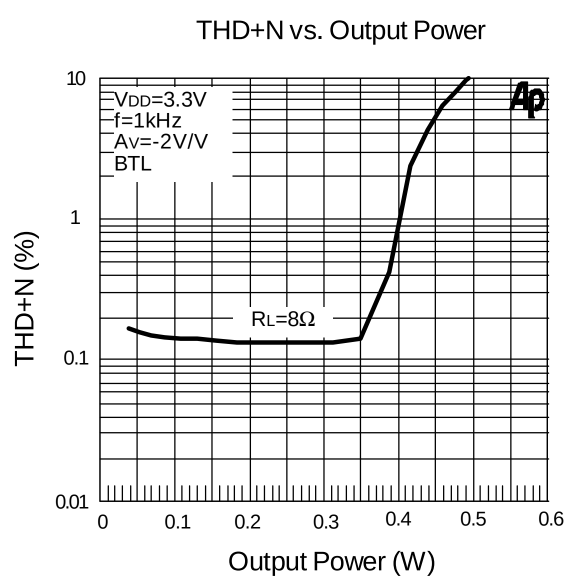
Typical Characteristics (Cont.)









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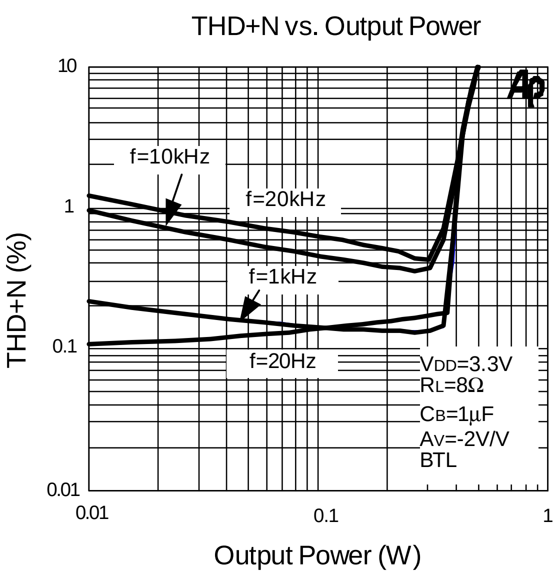

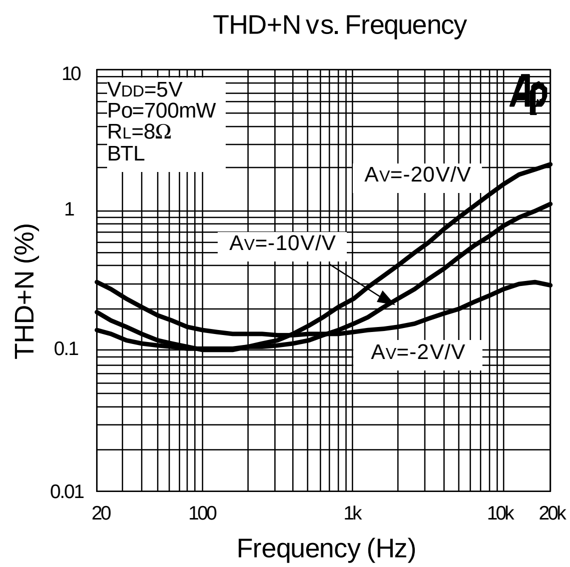

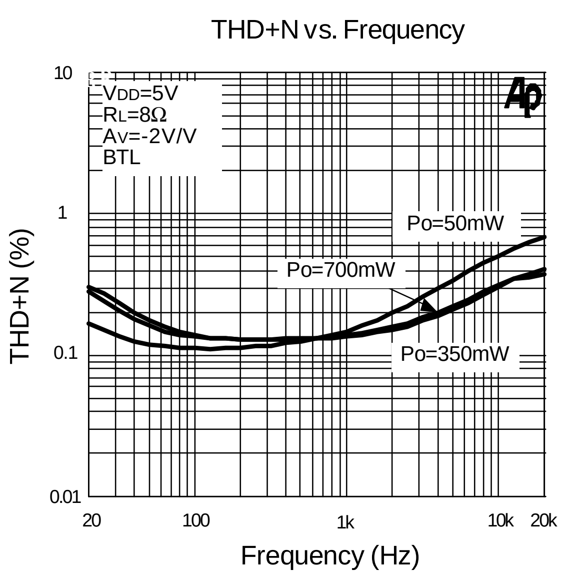

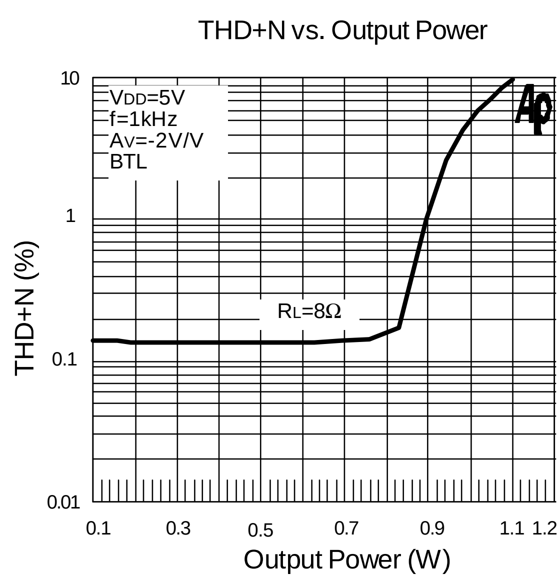

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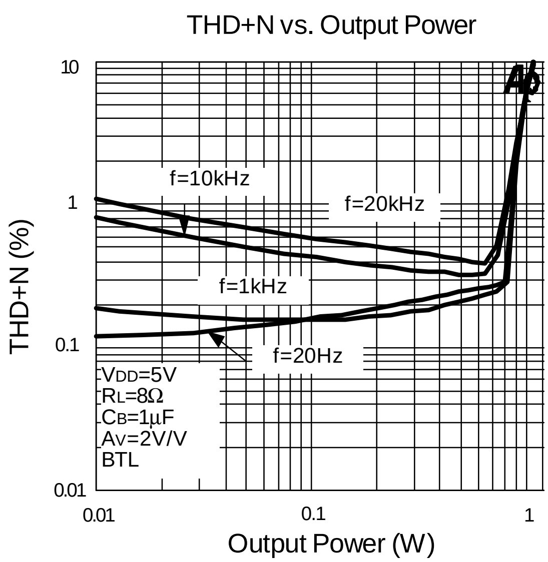
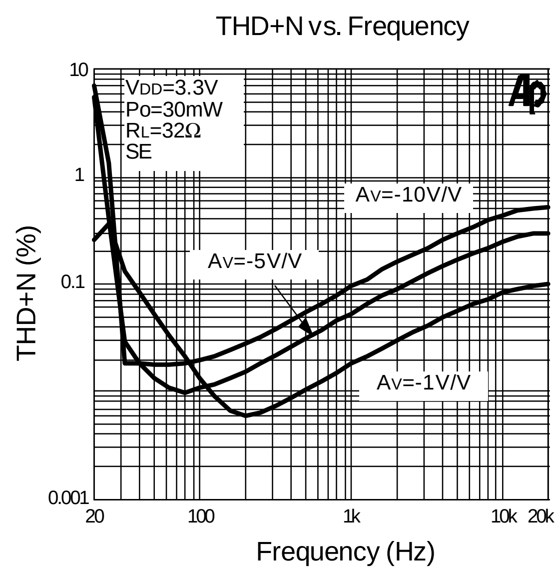
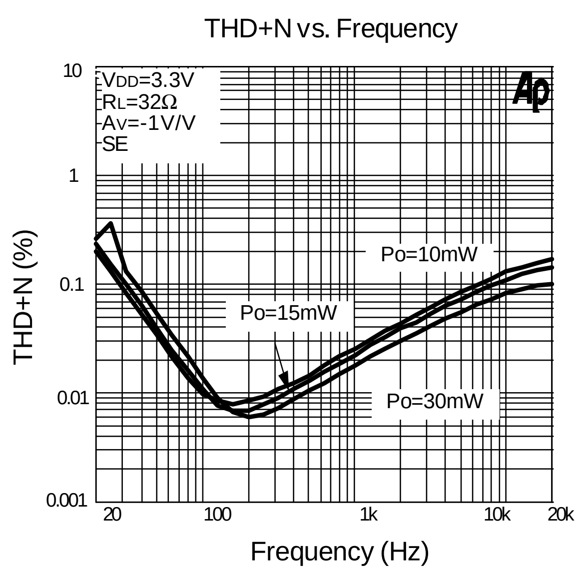
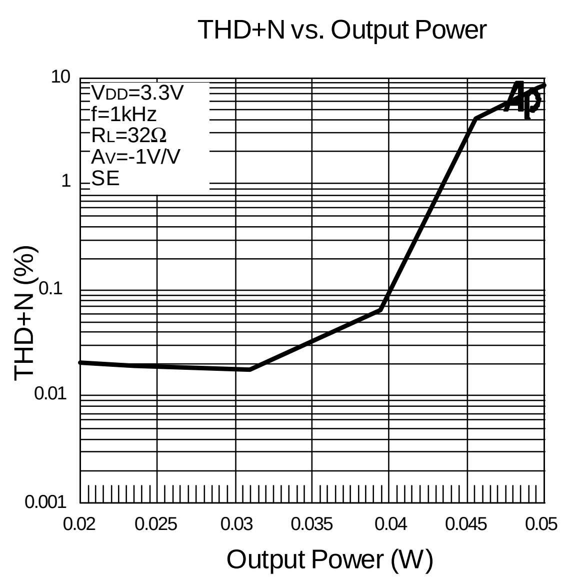
Typical Characteristics (Cont.)









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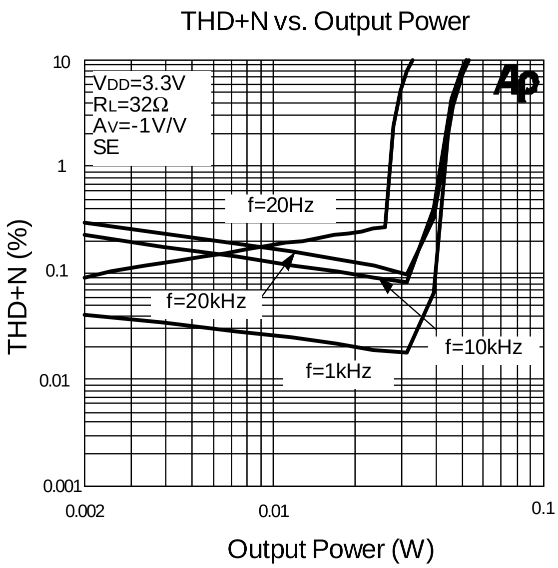

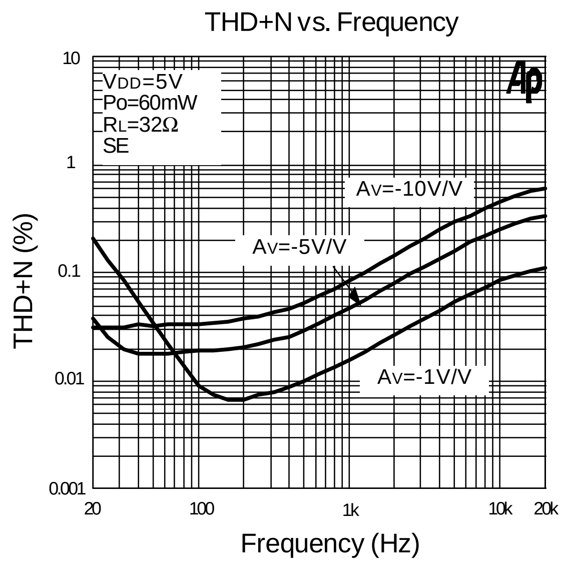

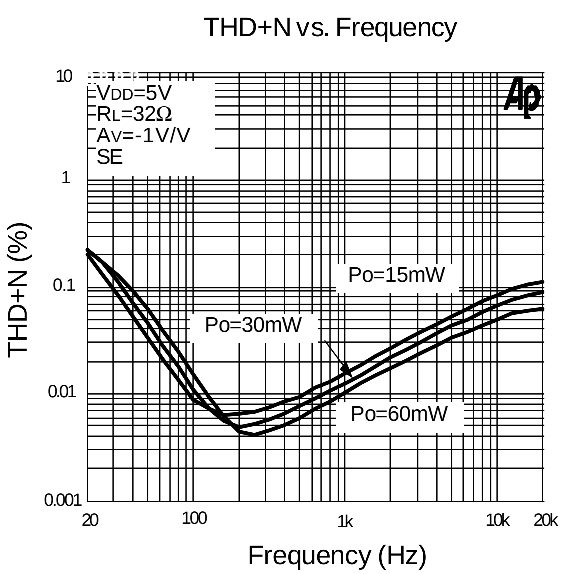

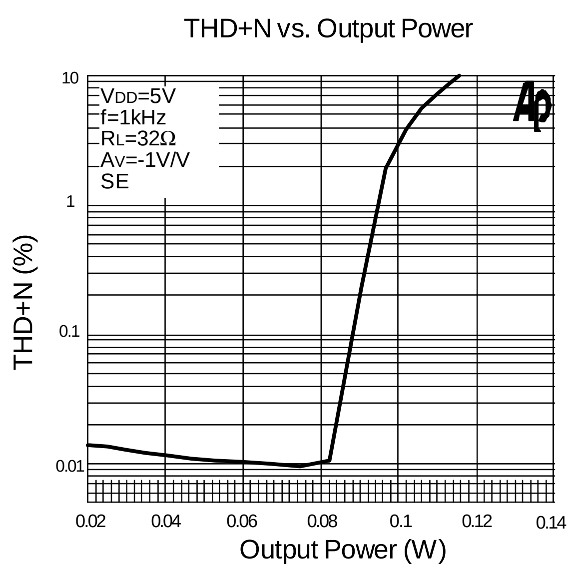

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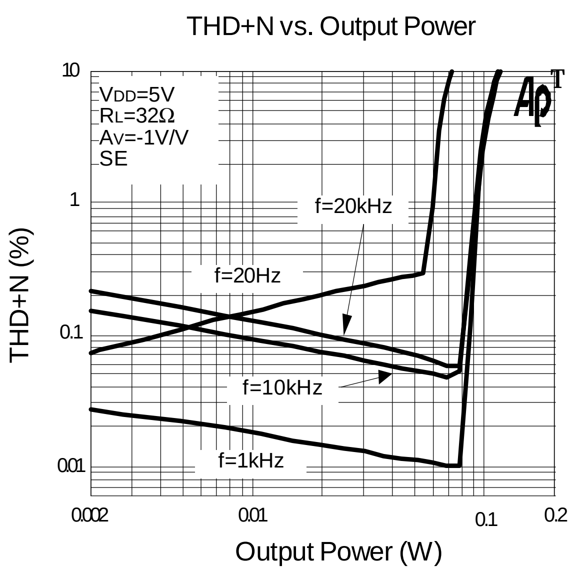
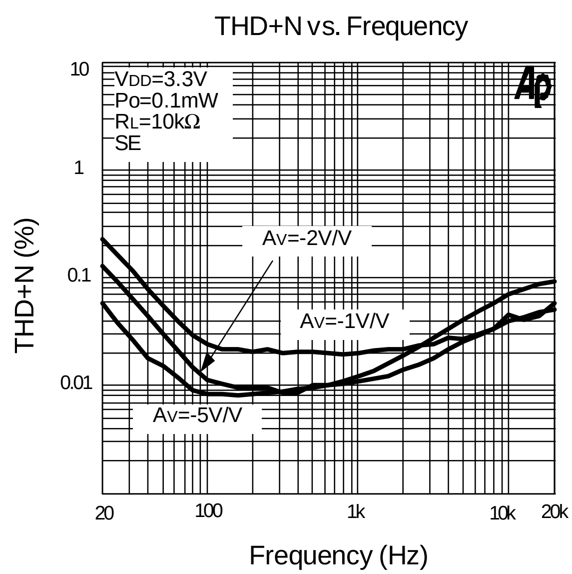
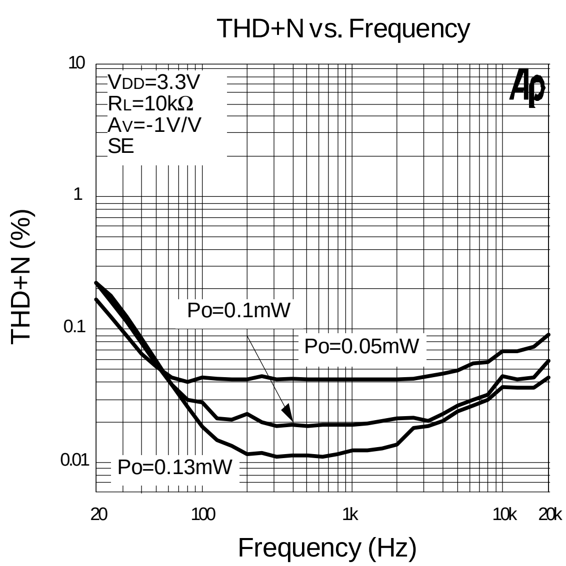
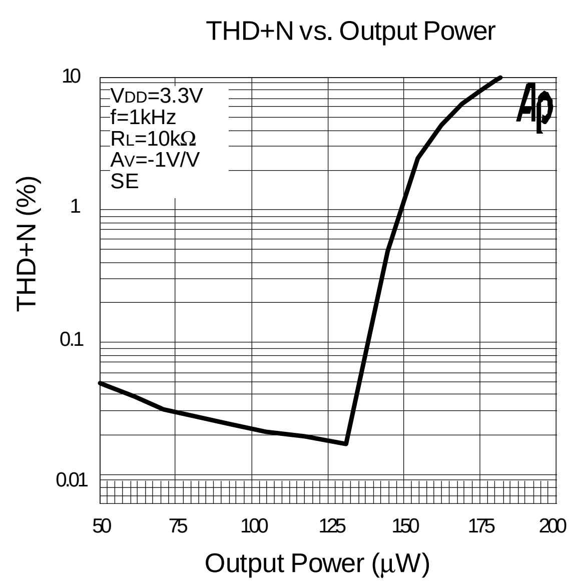


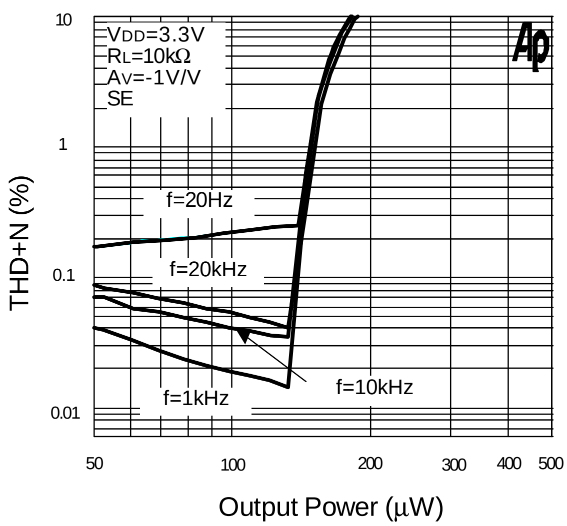




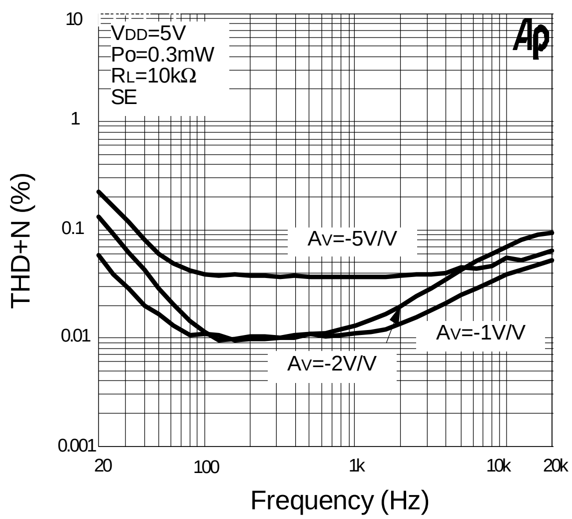


Typical Characteristics (Cont.)

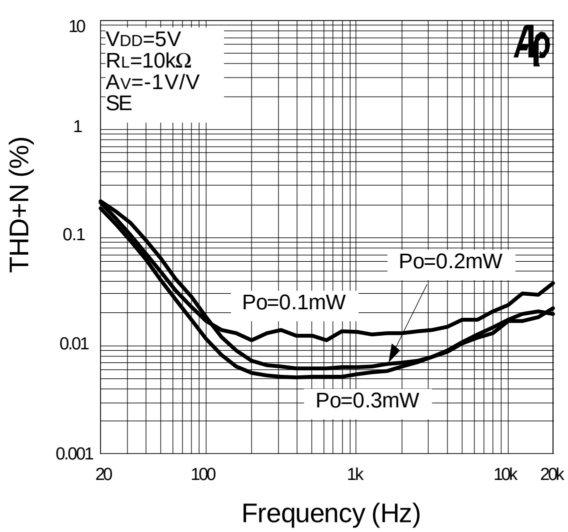
THD+N vs. Output Power



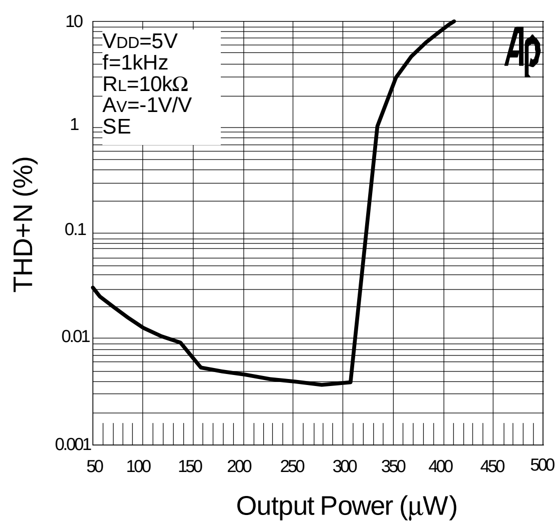
THD+N vs. Frequency



THD+N vs. Frequency

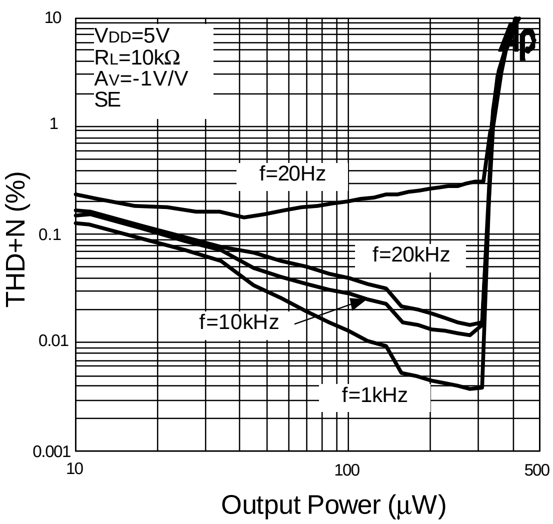


THD+N vs. Output Power

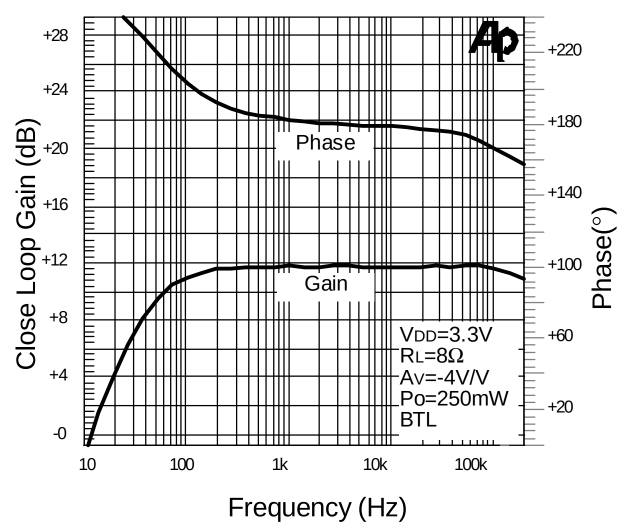


Typical Characteristics (Cont.)

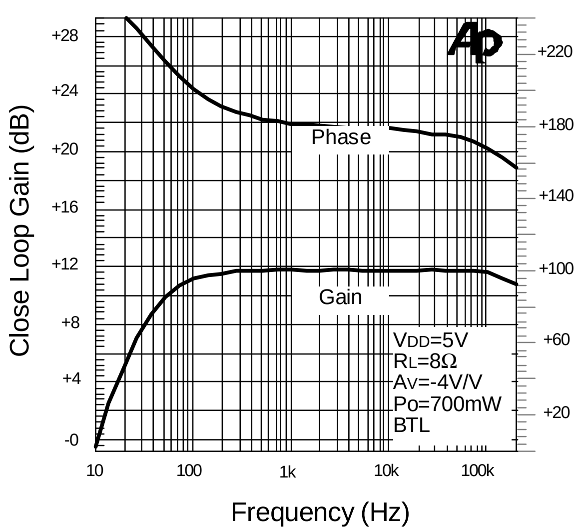
THD+N vs. Output Power



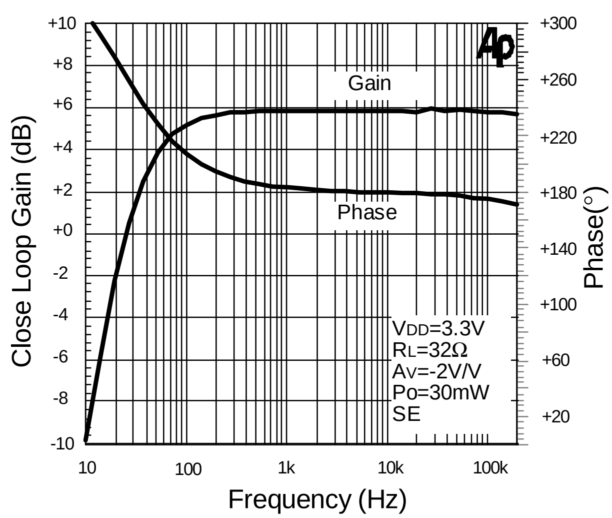
Close Loop Gain and Phase vs. Frequency



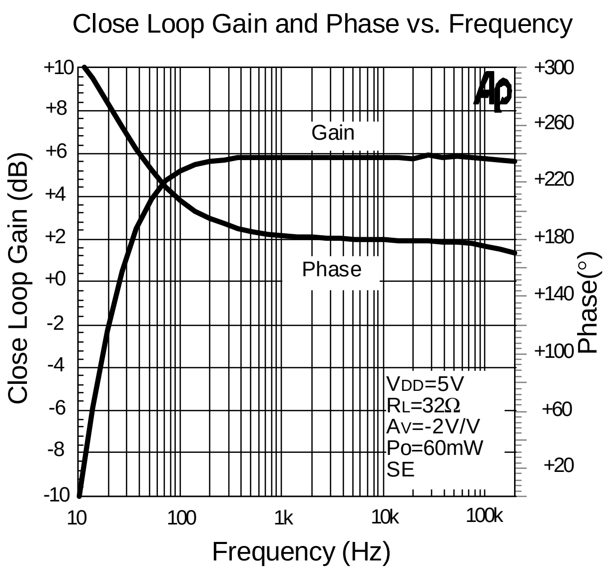
Close Loop Gain and Phase vs. Frequency

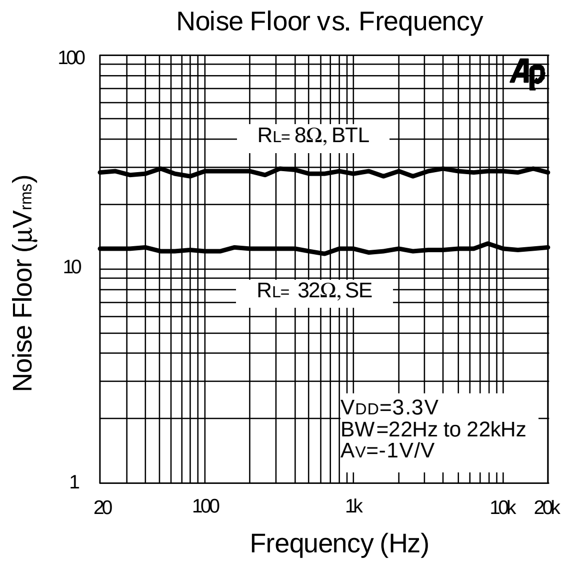


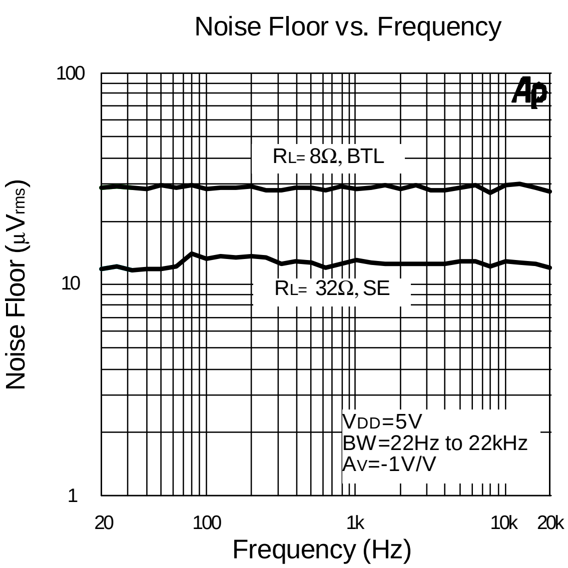
Close Loop Gain and Phase vs. Frequency

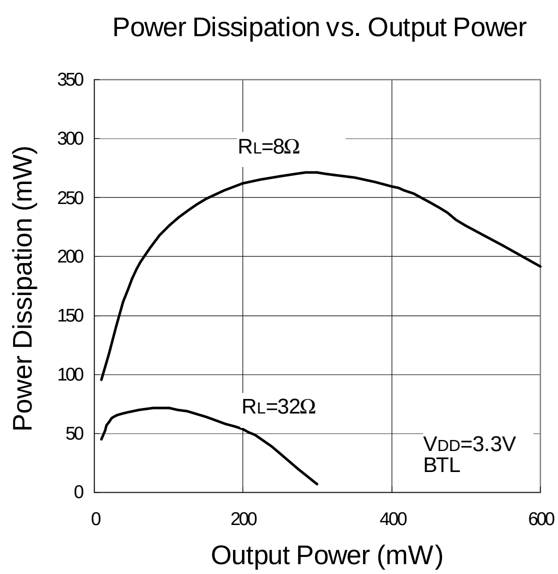


Typical Characteristics (Cont.)

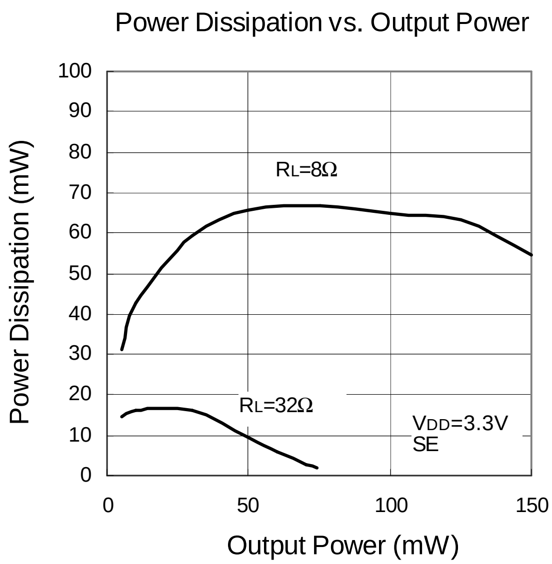


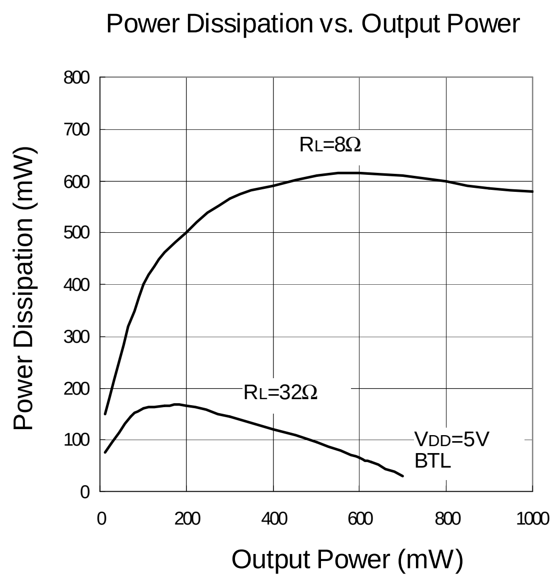


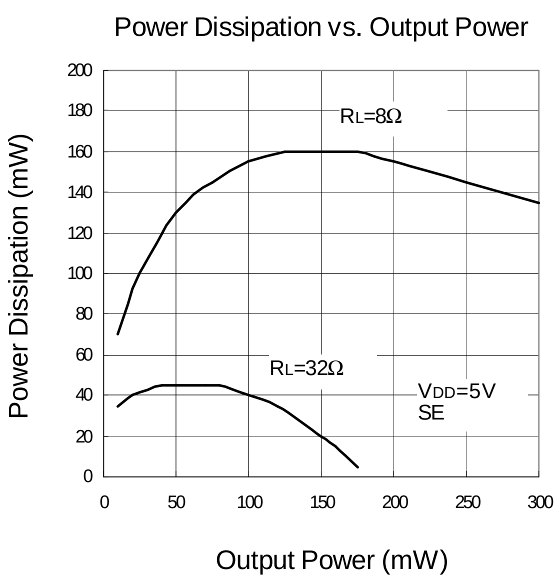




Typical Characteristics (Cont.)







Application Descriptions

BTL Operation

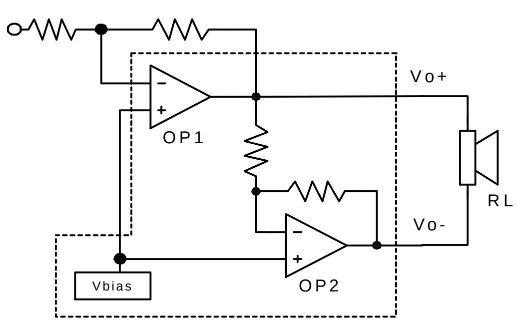


Figure1:
APA0710/1 power amplifier internal configuration

The power amplifier OP1 gain is setting by external gain setting, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs Vo+ and Vo-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

Four times the output power is possible as compared to a SE amplifier under the same conditions. A BTL configuration, such as the one used in APA0710, also creates a second advantage over SE amplifiers. Since the differential outputs, Vo+, Vo- are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

The rules described still hold with the addition of the following relationship :

$$\frac{1}{C_{bypass}\times 80k\Omega} \leq \frac{1}{(R_I+R_F)\times C_I} << \frac{1}{R_L C_C} \qquad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation (for APA0710 only)

The ability of the APA0710 to easily switch between BTL and SE modes is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA0710, two separate amplifiers drive Vo+ and Vo- (see Figure 2). The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives Vo-.

- When SE/$\overline{\text{BTL}}$ is held low, the OP2 is turn on and the APA0710 is in the BTL mode.
- When SE/$\overline{\text{BTL}}$ is held high, the OP2 is in a high output impedance state, which configures the APA0710 as SE driver from Vo+. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{\text{BTL}}$ input can be a logic-level TTL

Application Descriptions (Cont.)

Output SE/$\overline{\text{BTL}}$ Operation (for APA0710 only)

source or a resistor divider network or the mono headphone jack with switch pin as shown in Application Circuit.

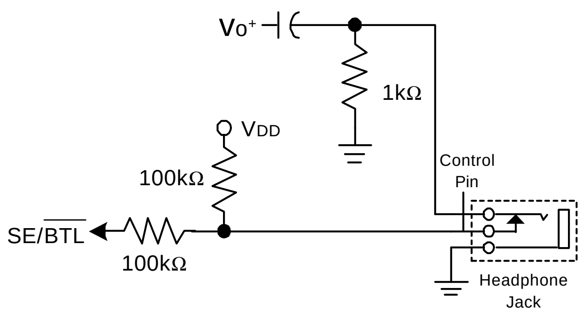


Figure 2: SE/$\overline{\text{BTL}}$ input selection by phonejack plug

In Figure 2, input SE/$\overline{\text{BTL}}$ operates as follows :

When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high and enables the SE mode.

When this input goes high level, the Vo- amplifier is shutdown causing the speaker to mute. The Vo+ amplifier then drives through the output capacitor (C_C) into the headphone jack.

When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{\text{BTL}}$ pin, enabling the BTL function.

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the follow equation :

$$F_C(\text{highpass}) = \frac{1}{2\pi R_i C_i} \qquad (2)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 100kΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as follow :

$$C_i = \frac{1}{2\pi R_i f_C} \qquad (3)$$

Consider to input resistance variation, the Ci is 0.04µF so one would likely choose a value in the range of 0.1µF to 1.0µF.

A further consideration for this capacitor is the leakage path from the input source through the input network (Ri+Rf, Ci) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, Cbypass

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor will improve PSRR due to increased half-supply stability. Typical application employ a 5V regulator with 1.0µF and a 0.1µF bypass as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA0710/1. The selection of

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Application Descriptions (Cont.)

Effective Bypass Capacitor, Cbypass (Cont.)

bypass capacitors, especially Cbypass, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (4) should be maintained.

$$\frac{1}{Cbypass \times 80kO} << \frac{1}{(R_I + R_F) \times C_I} \quad (4)$$

The bypass capacitor is fed from a 80kΩ resistor inside the amplifier. Bypass capacitor, Cbypass, values of 0.1µF to 2.2µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start up time. It is determined in the following equation :

$$Tstart\ up = 5 \times (Cbypass \times 80k\Omega) \quad (5)$$

Output Coupling Capacitor, Cc (for APA0710 only)

In the typical single-supply (SE) configuration on a APA0710, an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation.

$$F_C(highpass) = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load.

Power Supply Decoupling, Cs

The APA0710/1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA0710/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of Ci will also affect turn-on pops (refer to Effective Bypass Capacitance). The bypass voltage rise up should be slower than input bias voltage.

Although the bypass pin current source cannot be modified, the size of Cbypass can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cbypass, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the

Application Descriptions (Cont.)

Optimizing Depop Circuitry (Cont.)

size of Cbypass and the turn-on time.

In a SE configuration, the output coupling capacitor, C_C, is of particular concern. This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_C, the time constant can be relatively large.

In the most cases, choosing a small value of Ci in the range of 0.33μF to 1μF, Cbypass being equal to 1μF should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the APA0710/1 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the Shutdown pin for APA0710 and a logic low on the $\overline{\text{Shutdown}}$ pin for APA0711.

The trigger point between a logic high and logic low level is typically $0.4V_{DD}$. It is best to switch between ground and the supply voltage V_{DD} to provide maximum device performance.

By switching the Shutdown/$\overline{\text{Shutdown}}$ pin to high level/ low level, the amplifier enters a low-current state, I_{DD} for APA0710/1. APA0710/1 are in shutdown mode. On normal operating, APA0710's Shutdown pin pull to low level and APA0711's $\overline{\text{Shutdown}}$ pin should pull to high level to keeping the IC out of the shutdown mode. The Shutdown/$\overline{\text{Shutdown}}$ pin should be tied to a definite voltage to avoid unwanted state changes.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \qquad (7)$$

Where :

$$P_O = \frac{V_{O,RMS} \times V_{O,RMS}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{O,RMS} = \frac{V_P}{\sqrt{2}} \qquad (8)$$

$$P_{SUP} = V_{DD} \times I_{DD,AVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \qquad (9)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \qquad (10)$$

Po (W)	Efficiency (%)	V_P(V)	P_D (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45*	0.28

*High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 3.3V/8Ω BTL Systems.

Table 1 employs equation10 to calculate efficiencies for three different output power levels when load is 8Ω.

The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a mono 900mW audio system with 8Ω loads and a 5V supply, the maximum draw on the

Application Descriptions (Cont.)

BTL Amplifier Efficiency (Cont.)

power supply is almost 1.5W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation10, V_{DD} is in the denominator.

This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation11 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \qquad (11)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \qquad (12)$$

Since the APA0710/1 is a mono channel power amplifier, the maximum internal power dissipation is equal to the both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA0710/1 does not require extra heatsink. The power dissipation from equation12, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation13 :

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \qquad (13)$$

For MSOP-8-P package with and SOP-8 without thermal pad, the thermal resistance (θ_{JA}) is equal to 50°C/W and 160°C/W, respectively.

Since the maximum junction temperature ($T_{J,MAX}$) of APA0710/1 are 170°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation13. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the APA0710/1 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA0710/1 8Ω will go into thermal shutdown when driving a 8Ω load.

The thermal pad on the bottom of the APA0710/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 6 to 10 vias of 12 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA0710/1 junction temperature below the thermal shutdown temperature (170°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

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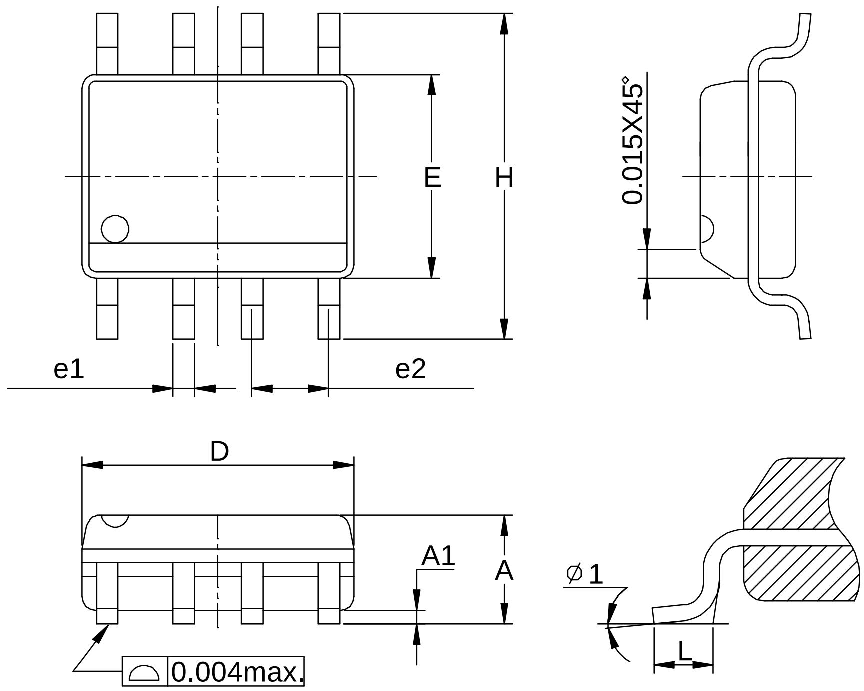
Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	0°	8°	0°	8°

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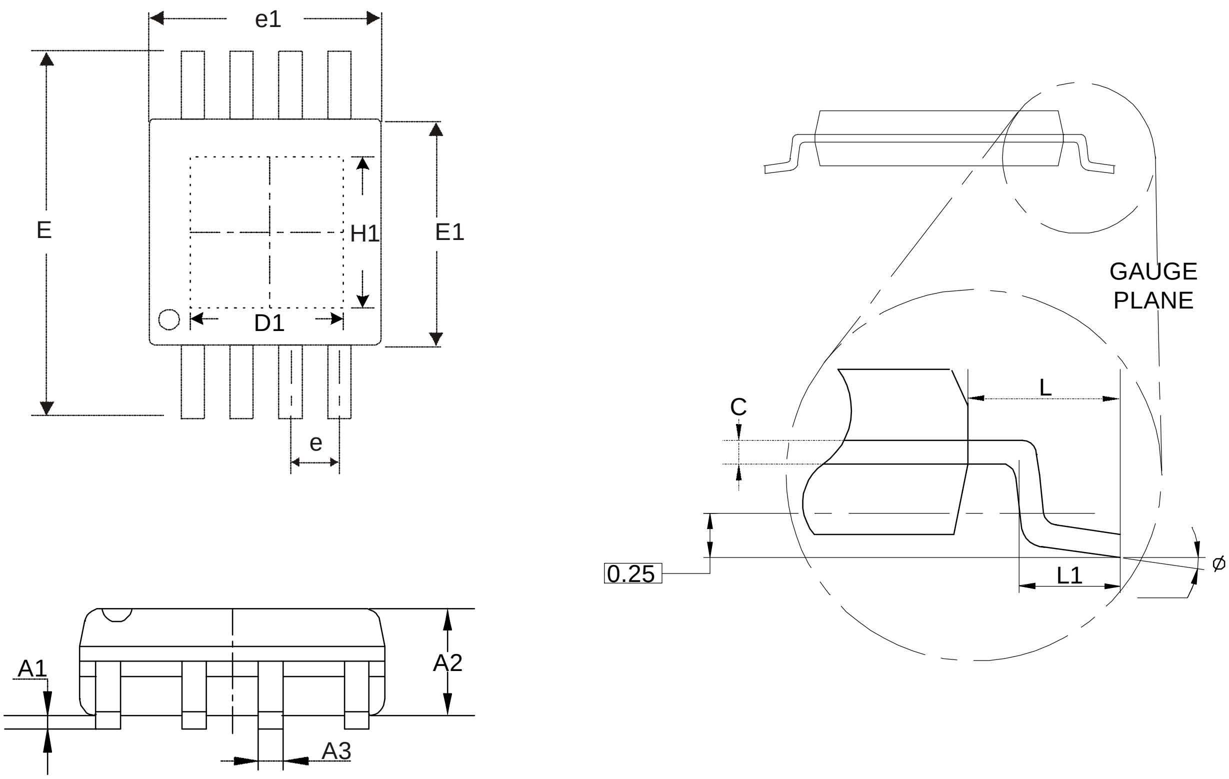
Packaging Information

MSOP-8-P



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A1	0.06	0.15	0.002	0.006
A2	0.86 TYP		0.34 TYP	
A3	0.25	0.4	0.01	0.0126
C	0.13	0.23	0.005	0.009
e	0.65 TYP		0.0256 TYP	
e1	2.90	3.1	0.114	0.122
E	4.8	5.0	0.189	0.197
E1	2.90	3.1	0.114	0.122
D1	2.146 REF		0.0845 REF	
H1	1.740 REF		0.0685 REF	
L	0.9	1.0	0.036	0.039
L1	0.45	0.65	0.018	0.026
ϕ	6°		6°	

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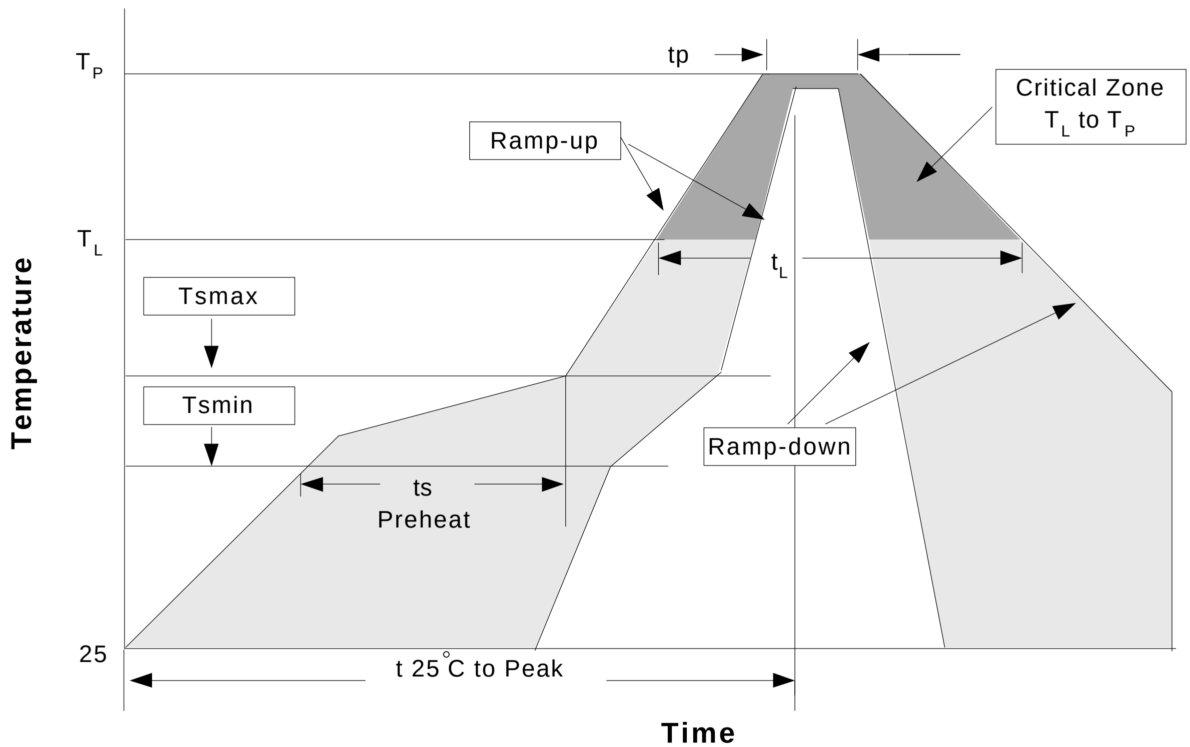
Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

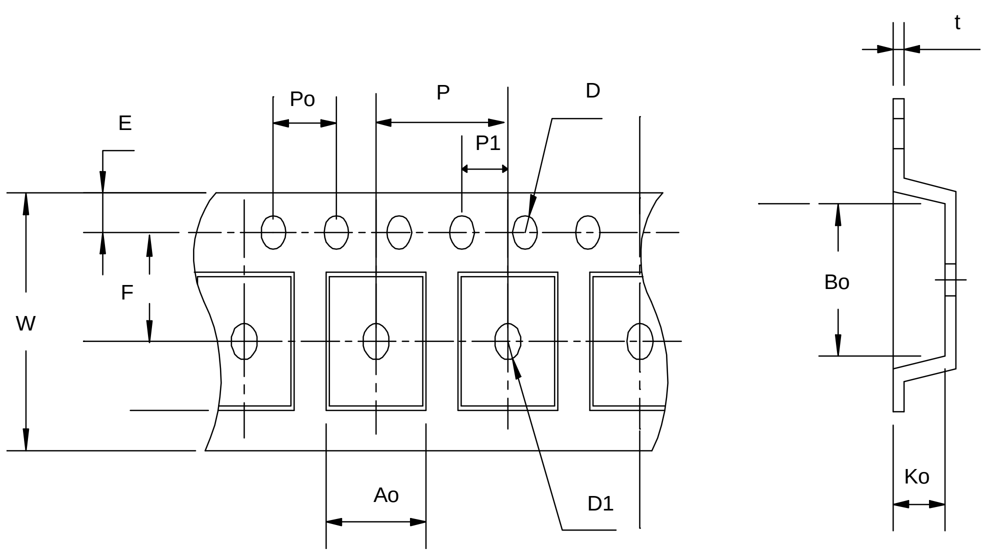
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



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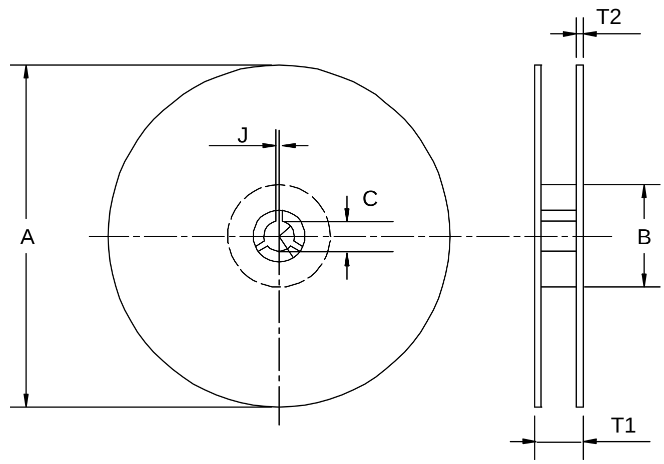
Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
M/SOP-8	330±1	62 ± 1.5	12.75 + 0.1 5	2 + 0.5	12.4 +0.2	2± 0.2	12 + 0.3 - 0.1	8± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.1	1.55±0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500
MSOP- 8	12	9.3	3000

Customer Service

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